<u>**AMENDMENTS TO THE CLAIMS**</u>

This listing of claims will replace all prior versions and listing of claims in the application.

<u>**Listing of Claims**</u>

1.   (Previously Presented)   A semiconductor device comprising:

a memory block addressed by a binary address of NA bits; and

a defect address storing circuit including ND (ND = $2^{\wedge}$NA) storage elements for storing

NS (NS = two or more) defect addresses in relation to a plurality of defects in the memory

block,

wherein the NS defect addresses from said binary address of NA bits are addresses

which are different from each other, and

each of the ND storage elements stores one bit.

2.   (Previously Presented)   A semiconductor device according to claim 1,

wherein an initial value of each of the ND storage elements is in a first logical state and

the NS storage elements in the ND storage elements are programmed into a second logical

state, thereby storing the NS defect addresses.

3.   (Previously Presented)   A semiconductor device according to claim 1,

wherein each of the NS defect addresses is expressed by a decoded address of ND bits,

wherein one bit of the decoded address of ND bits is in a second logical state and the

other bits are in a first logical state, which is different from said second logical state, and

wherein the bits in the second logical state of the NS defect addresses are sequentially

programmed into the ND storage elements in accordance with the order starting from an

address having a first value to an address having a second value larger than said first value.

4.   (Original)   A semiconductor device according to claim 1,

wherein $NS > (2^{NA})/(NA + 1)$ is satisfied.

5.   (Original)   A semiconductor device according to claim 1,

wherein each of the plurality of memory circuits includes a plurality of memory cells

provided at intersecting points of a plurality of word lines and a plurality of bit lines and

wherein the number of the plurality of memory circuits is ND.

6.   (Original)   A semiconductor device according to claim 5, further comprising:

a flexible column redundancy circuit for repairing a defect in the bit lines in the

plurality of memory circuits,

wherein the defect address storing circuit is included in the flexible column redundancy

circuit, and

wherein the ND storage elements store addresses of the plurality of memory circuits

relating to a defect.

7.   (Previously Presented)   A semiconductor device according to claim 1,

wherein each of the ND storage elements is a fuse circuit for storing <u>a</u> first logical state

as an initial value and storing a second logical state by being programmed.

8-35.   (Canceled)